IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application : **10/023,117**

Applicant(s) : **PEREIRA et al.**

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Examiner : **ELLIS, Richard L.**

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Title: **DATA PROCESSING DEVICE WITH A CONFIGURABLE FUNCTIONAL UNIT AND LOGIC REUSE ACROSS DIFFERENT CUSTOMIZED OPERATIONS**

Mail Stop: **APPEAL BRIEF - PATENTS**
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 7 June 2007, finally rejecting claims 1-20 of the subject application.

This paper includes (each beginning on a separate sheet):

1. **Appeal Brief;**
2. **Claims Appendix;**
3. **Evidence Appendix; and**
4. **Related Proceedings Appendix.**

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending in the application.

Claims 1-20 stand rejected by the Examiner under 35 U.S.C. 102(b).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection in the Office Action dated 7 June 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a data processing device with configurable functional units that receive data from source registers and provides processed data to destination registers (Applicants' FIG. 1; page 4, lines 7-10). As in conventional devices, a connection circuit (162) selectively routes bits from the source registers (12) to the inputs of logic blocks (164) (page 2, lines 19-21). The logic blocks (164) produce result bits corresponding to the configured function and the selected order of the input bits (page 5, lines 1-3). In accordance with this invention, an additional connection circuit (166) is provided to selectively route the result bits from the logic blocks (164) to the destination registers (12) (page 2, line 30 – page 3, line 3; page 4,

lines 21-22; page 5, line 3). By providing selective routing of bits on both the inputs and outputs of the logic blocks, programming efficiency and flexibility are significantly enhanced, including the reuse of logic across customized operations (page 3, lines 15-18 and 26-28).

As claimed in independent claim 1, the invention comprises a data processing device (FIG. 1) configured according to a device configuration (169) so as to be capable of executing a program comprising an instruction (10), the device comprising:

a configurable functional unit (16) for executing the instruction according to a configurable function (169) that is configured outside the instruction, the configured function including an input ordering instruction (169 to 162), a configured logic function (169 to 164), and an output ordering instruction (169 to 166) (page 4, lines 23-25),

the configurable functional unit including:

a unit input (160) for inputting a plurality of input bits of one or more source registers (12) specified by the instruction (10) (page 4, lines 19-21),

a unit output (168) for outputting a plurality of output bits to a destination register (12) specified by the instruction (10) (page 4, lines 21-23),

a first programmable connection circuit (162) that is configured to receive the plurality of input bits and selectively route the input bits to provide a set of logic input bits, based on the input ordering instruction (page 5, lines 9-12),

a plurality of independent configurable logic blocks (164) for performing programmable logic operations to produce a set of logic output bits corresponding to the configured logic function being applied to the set of logic input bits (page 5, lines 13-23), and

a second programmable connection circuit (166) that is configured to receive the set of logic output bits and selectively route the logic output bits to provide the plurality of output bits, based on the output ordering instruction (page 6, lines 3-10).

As claimed in independent claim 5, the invention comprises a method (FIG. 3) of programming a configurable processing device (FIG. 1) according to a device configuration to perform a processing task, wherein the device includes a configurable processing unit that includes one or more programmable logic blocks, the method comprising:

identifying (33) a special complex of operations that occurs in the task and requires one or more operand data words and produces a result data word (page 7, lines 30-32);

searching (34-35) for an assignment of logic operations for producing different bits of the result data word to different ones of the programmable logic blocks (page 8, lines 7-11), so that the logic operations for producing a subset of the bits of the result data word that, if implemented together in one of the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks (page 8, lines 17-29);

programming (36) each of the programmable logic blocks to perform the logic operations for the bits of the result data word assigned to it (page 9, lines 10-12; page 8, lines 20-22);

programming (36) a first connection circuit to the programmable logic blocks so as to perform a first routing of bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations (page 9, lines 10-12; page 8, line 33 – page 9, line 2); and

programming (36) a second connection circuit subsequent to the logic blocks so as to perform a second routing of outputs of the programmable logic blocks to bits of the result data word to which the programmable logic blocks are assigned (page 9, lines 10-12; page 8, lines 30-32).

As claimed in independent claim 6, the invention comprises a method of executing a program with a processing device (FIG. 1) with a configurable functional unit (16) according to a device configuration, the method comprising:

inputting one or more words of one or more operands of a program instruction (10) into the configurable functional unit (16), each word including a plurality of bits (page 4, lines 26-29);

selectively coupling (162) the bits of the words of the operands to inputs of logic blocks, dependent on a configured function of the configurable functional unit (page 5, lines 9-12);

performing programmable logic operations (164) to implement the configured function to provide an output word that includes a plurality of bits (page 5, lines 13-25);

selectively coupling (166) bits of the output word to bits of a result word, dependent on the configured function (page 6, lines 3-10); and

outputting (168) the result word to a destination (12) identified in the program instruction (page 5, lines 1-3).

As claimed in independent claim 7, the invention comprises a data processing device (FIG. 1) comprising:

a register file (12) that includes a plurality of registers, each register including a word, each word including a plurality of bits in a first bit order (page 4, lines 7-10), and

at least one configurable function units (16) that is dynamically configurable to effect different functions at different times, based on received configuration data (169) (page 5, lines 4-8), the at least one configurable function unit (16) including:

a first connection circuit (162) that is configured to receive one or more words from the plurality of registers (12), and to provide one or more words of bits in a second bit order based on the received configuration data (169) (page 5, lines 9-12),

one or more programmable logic blocks (164) that are configured to receive the one or more words in the second bit order from the first connection circuit, and to provide an output word of bits in a first output bit order based on the received configuration data (169) (page 5, lines 13-27), and

a second connection circuit (166) that is configured to receive the output word and to provide therefrom a word of bits in a second output bit order that is stored in a destination register of the plurality of registers based on the received configuration data (169) (page 6, lines 3-10).

As claimed in independent claim 13, the invention comprises a device (FIG. 1) comprising:

a processor (16) that is configured to execute instructions that identify: an operation, one or more source registers, and a destination register, each register including a word that includes a plurality of bits (page 4, line 32 – page 5, line 3), the processor including:

a first connection circuit (162) that receives (160) a word from a source register of the one or more source registers (12) and provides an operand word that includes a plurality of bits that are arranged in a bit order based on a programmed set of configuration data (169) corresponding to the operation (page 5, lines 9-12),

a configurable function circuit (164) that provides a result word based on the operand word and the programmed set of configuration data (169) (page 5, lines 13-27), and

a second connection circuit (166) that receives the result word and provides an output word for storing (168) in the destination register (12) that includes a plurality of bits that are arranged in a bit order based on the programmed set of configuration data (page 6, lines 3-10).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-20 stand rejected under 35 U.S.C. 102(b) over Abbott (USP 6,006,321).

VII. ARGUMENT

Claims 1-20 stand rejected under 35 U.S.C. 102(b) over Abbott

MPEP 2131 states:

> "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The ***identical invention*** must be shown in as ***complete detail*** as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1-4

Claim 1, upon which claims 2-4 depend, claims a data processing device that includes a unit output for outputting a plurality of output bits to a destination register specified by an instruction, and a programmable connection circuit that receives a set of logic output bits and selectively routes the logic output bits to provide the plurality of output bits to the destination register based on an output ordering instruction.

Abbott fails to teach an output ordering instruction, and fails to teach routing logic output bits to a destination register specified in an instruction based on the output ordering instruction.

The final Office action asserts that:

> "the claim language [of claim 1] simply requires a plurality of configurable logic blocks that produce an output, and a programmable connection circuit that receives the outputs from the logic blocks and that itself provides a rearranged output" (Final Office action, page 2, lines 3-6).

The applicants respectfully disagree with this assertion, and respectfully maintain that this abbreviated interpretation ignores many of the elements of the applicants' claim, and is inconsistent with the requirements of MPEP 2131, and inconsistent with the standards upheld by the Board of Patent Appeals and Interferences:

> "To meet [the] burden of establishing a prima facie case of anticipation, the examiner must explain how the rejected claims are anticipated by pointing out where ***all*** of the specific limitations recited in the rejected claims are found in the prior art relied upon in the rejection." *Ex Parte Naoya Isoda*, Appeal No. 2005-2289, Application 10/064,508 (BPAI Opinion October 2005).

Using this abbreviated interpretation of the applicants' claim, the Office action fails to identify where Abbott teaches an output ordering instruction, and fails to identify where Abbott teaches routing logic output bits to a destination register specified in an instruction based on such an output ordering instruction.

The Office action references Abbott's page 12, line 1 through page 13, line 43 for teaching the routing of logic output bits to the destination register. The applicants respectfully note, however, that the referenced text teaches an intermediate transposition circuit 410 within a bank 400 of a reduction network 212, the output of which is applied to a logic circuit 412 within the bank 400. The logic circuit 412 receives the output bits from the transposition circuit 410 and creates logic output bits that are output from the bank 400 of the reduction network 212, and optionally provided to a post processing unit 214. Abbott does not teach that the output of the transposition circuit 410 is provided to a destination register that is specified in an instruction, as specifically claimed in claim 1.

The Office action notes that:

> "the output from block 410 is processed through blocks 412 and 414, passed out of fig. 4 to block 214 of fig. 2, flows out of box 24 and forms the output of blocks 114, 116 of fig. 1, and is then stored in register bank 104 or 106."

And further asserts:

> "Accordingly, block 410 is 'providing the plurality of bits' that ultimately are stored in the register file." (Final Office action, page 2, lines 14-19.)

The applicants respectfully disagree with this assertion. The data that is stored in the register bank 104/106 is not the output of the transposition circuit 410. The output of the transposition circuit 410 is used as an input to a block 412 that performs a logic operation on this input to produce a logic output that differs from the output of block 412. Block 410 does not provide the bits "that ultimately are stored in the register file" as asserted in the final Office action.

Using the interpretation advocated by the Examiner, any and all of the elements within Abbott's data path, including the original source registers, qualify as elements that are "[a]ccordingly... 'providing the plurality of bits' that ultimately are stored in the register file." Such an interpretation renders the claimed limitation of "selectively [routing] the logic output bits to provide the plurality of output bits [that are output to the destination register], based on the output ordering instruction" (claim 1, last two lines) meaningless, and is inconsistent with the principles that have been repeatedly upheld by the Board of Patent Appeals and Interferences:

> "there must be ***no difference*** between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991)." *Ex Parte Naoya Isoda*, op cit.

One of skill in the art would not consider an intermediate transposition circuit that outputs bits to subsequent internal logic circuits and further processing units, as taught by Abbott, to be identical or equivalent to a connection circuit that selectively routes logic output bits to a destination register that is specified in an instruction based on an output ordering instruction, as claimed by the applicants.

The Office action fails to identify where Abbott teaches an output ordering instruction, and fails to identify where Abbott teaches routing logic output bits to provide a plurality of output bits to a destination register specified in an instruction based on such an output ordering instruction, as specifically claimed in claim 1. Accordingly, the applicants respectfully maintain that the rejection of claims 1-4 under 35 U.S.C. 102(b) over Abbott is unfounded, per MPEP 2131, and should be reversed by the Board.

Claim 5

Claim 5 claims a method that includes identifying a special complex of operations that occurs in the task and requires one or more operand data words and produces a result data word, programming a first connection circuit to perform a routing of bits of an operand of a special instruction to the programmable logic blocks, and programming a second connection circuit to perform a routing of outputs of the programmable logic blocks to bits of the result data word.

As noted above, Abbott does not teach programming a connection circuit to perform a routing of outputs of a programmable logic blocks to bits of a result data word that is identified in an operation that occurs in a task. The output of Abbott's block 410 is not a result data word that is identified in an operation that occurs in a task, as claimed in claim 5.

Accordingly, the applicants respectfully maintain that the rejection of claim 5 under 35 U.S.C. 102(b) over Abbott is unfounded, per MPEP 2131, and should be reversed by the Board.

Claim 6

Claim 6 claims a method that includes selectively coupling bits of words of operands to the inputs of logic blocks, dependent on a configured function, performing programmable logic operations to implement the configured function to provide an output word, and selectively coupling bits of the output word to bits of a result word dependent on the configured function and outputting the result word to a destination identified in the program instruction.

The Office action asserts that Abbott's element 410 selectively couples bits of an output word to bits of a result word dependent on a configured function, but fails to identify where Abbott teaches outputting this result word to a destination identified in a program instruction. As noted above, Abbott's element 410 is an intermediate module whose output is coupled to further logic blocks within a bank 400 of Abbott's reduction network 212. Abbott's element 410 does not output its result to a destination identified in a program instruction as specifically claimed in claim 6.

Because the Office action fails to identify where Abbott teaches each of the elements of claim 6, the applicants respectfully maintain that the rejection of claim 6 under 35 U.S.C. 102(b) over Abbott is unfounded, per MPEP 2131, and should be reversed by the Board.

Claims 7-12

The Office action relies upon the rejection of claims 1-6 to support the rejection of claims 7-12. As noted above, the applicants respectfully maintain that the rejection of claims 1-6 under 35 U.S.C. 102(b) over Abbott is unfounded, per MPEP 2131. Accordingly, the rejection of claims 7-12 based on the rejection of claims 1-6 should be reversed by the Board.

Specifically, and/or additionally, with regard to claim 7, upon which claims 8-12 depend, Abbott fails to teach a data processing device that includes a programmable logic block that provides an output word of bits in a first output bit order based on received configuration data, and a second connection circuit that receives the output word and provides therefrom a word of bits in a second output bit order that is stored in a destination register based on the received configuration data.

Claims 13-20

The Office action relies upon the rejection of claims 1-6 to support the rejection of claims 13-20. As noted above, the applicants respectfully maintain that the rejection of claims 1-6 under 35 U.S.C. 102(b) over Abbott is unfounded, per MPEP 2131. Accordingly, the rejection of claims 13-20 based on the rejection of claims 1-6 should be reversed by the Board.

Specifically, and/or additionally, with regard to claim 13, upon which claims 14-20 depend, Abbott fails to teach a device that includes a processor that executes instructions that identify an operation, one or more source registers, and a destination register, wherein the processor includes a configurable function circuit that provides a result word based on the operand word and a programmed set of configuration data, and a connection circuit that receives the result word and provides an output word for

storing in the destination register that includes a plurality of bits that are arranged in a bit order based on the programmed set of configuration data.

CONCLUSIONS

Because Abbott fails to teach a connection circuit that receives output bits from a configurable function circuit and selectively orders/routes the bits for storage in a specified destination register, the applicants respectfully request that the Examiner's rejection of claims 1-20 under 35 U.S.C. 102(b) be reversed by the Board, and the claims be allowed to pass to issue.

Respectfully submitted

/Robert M. McDermott/
Robert M. McDermott, Attorney
Registration Number 41,508
patents@lawyer.com
804-493-0707

Please direct all correspondence to:
Corporate Counsel
U.S. PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001

CLAIMS APPENDIX

1. A data processing device configured according to a device configuration so as to be capable of executing a program comprising an instruction, the device comprising

a configurable functional unit for executing the instruction according to a configurable function that is configured outside the instruction, the configured function including an input ordering instruction, a configured logic function, and an output ordering instruction,

the configurable functional unit including:

a unit input for inputting a plurality of input bits of one or more source registers specified by the instruction,

a unit output for outputting a plurality of output bits to a destination register specified by the instruction,

a first programmable connection circuit that is configured to receive the plurality of input bits and selectively route the input bits to provide a set of logic input bits, based on the input ordering instruction,

a plurality of independent configurable logic blocks for performing programmable logic operations to produce a set of logic output bits corresponding to the configured logic function being applied to the set of logic input bits,

a second programmable connection circuit that is configured to receive the set of logic output bits and selectively route the logic output bits to provide the plurality of output bits, based on the output ordering instruction.

2. The data processing device of claim 1, each logic block having a plurality of outputs, at least one of the output bits of the unit output being connectable exclusively to one of the outputs of each logic block, the second programmable connection circuit comprising a multiplexer for coupling the one of the outputs of a selected one of the logic blocks to the at least one of the output bits of the unit output.

3. The data processing device of claim 1, each logic bock having a plurality of outputs, each of the output bits of the unit output being connectable exclusively to a respective one of the outputs of each logic block, the second programmable connection circuit comprising a respective multiplexer for each particular bit of the unit output, for coupling the respective one of the outputs of a selected one of the logic blocks to the particular output bit of the unit output.

4. The data processing device of claim 1, either the first programmable connection circuit or the second programmable connection circuit having a fixed, unprogrammable connection to an input or output of one of the independent configurable logic blocks and a programmable connection to a remainder of the inputs and outputs.

5. A method of programming a configurable processing device according to a device configuration to perform a processing task, wherein the device includes a configurable processing unit that includes one or more programmable logic blocks, the method comprising:

identifying a special complex of operations that occurs in the task and requires one or more operand data words and produces a result data word;

searching for an assignment of logic operations for producing different bits of the result data word to different ones of the programmable logic blocks, so that the logic operations for producing a subset of the bits of the result data word that, if implemented together in one of the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks;

programming each of the programmable logic blocks to perform the logic operations for the bits of the result data word assigned to it;

programming a first connection circuit to the programmable logic blocks so as to perform a first routing of bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations; and

programming a second connection circuit subsequent to the logic blocks so as to perform a second routing of outputs of the programmable logic blocks to bits of the result data word to which the programmable logic blocks are assigned.

6. A method of executing a program with a processing device with a configurable functional unit according to a device configuration, the method comprising:

inputting one or more words of one or more operands of a program instruction into the configurable functional unit, each word including a plurality of bits;

selectively coupling the bits of the words of the operands to inputs of logic blocks, dependent on a configured function of the configurable functional unit;

performing programmable logic operations to implement the configured function to provide an output word that includes a plurality of bits;

selectively coupling bits of the output word to bits of a result word, dependent on the configured function; and

outputting the result word to a destination identified in the program instruction.

7. A data processing device comprising:

a register file that includes a plurality of registers, each register including a word, each word including a plurality of bits in a first bit order, and

at least one configurable function units that is dynamically configurable to effect different functions at different times, based on received configuration data, the at least one configurable function unit including:

a first connection circuit that is configured to receive one or more words from the plurality of registers, and to provide one or more words of bits in a second bit order based on the received configuration data,

one or more programmable logic blocks that are configured to receive the one or more words in the second bit order from the first connection circuit, and to provide an output word of bits in a first output bit order based on the received configuration data,

a second connection circuit that is configured to receive the output word and to provide therefrom a word of bits in a second output bit order that is stored in a destination register of the plurality of registers based on the received configuration data.

8. The data processing device of claim 7, including an input unit that is configured to receive the one or more words from the plurality of registers, and to provide the one or more words to the first connection circuit.

9. The data processing device of claim 8, including an output unit that is configured to receive the one or more words from the second connection circuit, and to provide the one or more words to the destination register.

10. The data processing device of claim 7, including an output unit that is configured to receive the one or more words from the second connection circuit, and to provide the one or more words to the destination register.

11. The data processing device of claim 7, wherein source registers of the one or more words from the plurality of registers are identified in an instruction that effects execution of a current function of the at least one configurable function unit.

12. The data processing device of claim 7, wherein the destination register is identified in the instruction.

13. A device comprising:

a processor that is configured to execute instructions that identify: an operation, one or more source registers, and a destination register, each register including a word that includes a plurality of bits, the processor including:

a first connection circuit that receives a word from a source register of the one or more source registers and provides an operand word that includes a plurality of bits that are arranged in a bit order based on a programmed set of configuration data corresponding to the operation,

a configurable function circuit that provides a result word based on the operand word and the programmed set of configuration data,

a second connection circuit that receives the result word and provides an output word for storing in the destination register that includes a plurality of bits that are arranged in a bit order based on the programmed set of configuration data.

14. The device of claim 13, wherein the processor includes an input port that is configured to receive the word from the source register, and to provide the word to the first connection circuit.

15. The device of claim 14, wherein the processor includes an output port that is configured to receive the output word from the second connection circuit, and to provide the output word to the destination register.

16. The device of claim 13, wherein the processor includes an output port that is configured to receive the output word from the second connection circuit, and to provide the output word to the destination register.

17. The device of claim 13, wherein the processor includes one or more other function circuits that are configured to receive one or more words from the plurality of registers and provide one or more other result words to the plurality of registers.

18. The device of claim 13, including an instruction issue unit that is configured to provide the instructions to the processor.

19. The device of claim 18, including a configuration control circuit that is configured to provide the set of configuration data corresponding to the operand based on a configuration instruction from the instruction issue unit.

20. The device of claim 13, including a configuration control circuit that is configured to provide the set of configuration data corresponding to the operand.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.